UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/494,787 | 01/31/2000 | John A. Mount | SEA9274 | 3950 |

7590 11/05/2004

DAVID K LUCENTE
SEAGATE TECHNOLOGY LLC
INTELLECTUAL PROPERTY DEPT COL2LGL
389 DISC DRIVE
LONGMONT, CA 80503

| EXAMINER | |
|---|---|
| NGUYEN, MIKE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2182 | |

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/494,787 | MOUNT, JOHN A. |
| | Examiner | Art Unit |
| | Mike Nguyen | 2182 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Notices & Remarks*

1. Applicant's amendment 06/16/2004 in response to Examiner's Office Action has been reviewed. The following rejections now apply.

2. Claims 1-20 are pending for the examination.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Cloke (U.S. Pat. No. 6,411,452 B1).

As to claim 1, Cloke teaches in a storage system (fig. 1D) having a bus (fig. 1D element 36) operatively coupled to a first controller chip (fig. 1D element 32) and a first channel chip (fig. 1D element 26), the channel chip having several registers (see fig. 4 element 122), the storage system also having a storage medium (fig. 1D element 10) operatively coupled to the bus through a storage medium interface (fig. 1D element 22), a method for retrieving data record on a storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (fig. 1D col. 21 lines 57-63 wherein digital read data is conveyed to the controller 32 via a channel data bus that coupled to the bus 36 through the channel chip 26);

(b) updating some of the registers via the bus (fig. 5 col. 27 line 55 to col. 28 line 2); and

(c) retrieving a second portion of the record data via the bus (fig. 2B col. 27 lines 57-67 wherein storage medium 10 has plurality of zone bands. Therefore, it is inherently that a record data in another zone band is retrieved after the first record data).

As to claim 2, Cloke teaches the method of claim 1 in which the interface includes a read head (fig. 1A element 19 col. 8 line 19), further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium (col. 8 lines 20-32 wherein the read head is used to position the interface), between retrieving step (a) and (c).

As to claim 3, Cloke teaches the method of claim 2 in which the interface has a plurality of operating parameters that are modified in updating step (b) (col. col. 22 lines 5-7).

As to claims 4 and 5, Cloke teaches the storage system of claim 1 configured to perform the method of claim 1 in which the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value; and at least one mode-indicative value (see col. 25 lines 2-12).

As to claim 16, Cloke teaches a method comprising steps of:

(a) providing data via a bus (fig. 1D element 36 col. 21 lines 57-63 wherein digital read data is conveyed to a controller 32 via a channel data bus that coupled to the bus 36 through the channel chip 26);

(b) updating at least one register or parameter via the bus (fig. 5 col. 27 line 55 to col. 28 line 2); and

(c) providing data via the bus responsive to the updating (col. 27 line 67 to col. 28 line 2 wherein read or write operations in the new data zone band is provided via the bus 36 after the register or parameter is updated).

As to claims 17-18, Cloke teaches the bus is serial and parallel (col. 22 line 40 and col. 12 lines 20-21).

As to claim 19, Cloke teaches the method of claim 16 wherein the steps are controlled by a processor (see fig. 1D element 34).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloke in view of Bowes et al. (U.S. Pat. No. 5,828,856).

As to claim 6, Cloke teaches in a storage system (fig. 1D) having a disc (fig. 1D element 14) with at least two zones having zone identifiers Za and Zb (see fig. 2B elements 62, 64, Di, Si col. 25-29), an interface (fig 1D element 22) configured to read data in zone Za, a target segment in zone Zb, a value table indexed by zone identifiers (col. 32 lines 38-47), a controller (fig. 1D

element 32), a microprocessor (fig. 1D element 34) coupled to the controller, and several read channel registers each containing value (fig. 1D element 26 and fig. 4 element 122), a method comprising steps of:

(a) retrieving via the controller several values indexed by zone identifier Zb (col. 30 lines 33-53 and col. 32 lines 38-47 );

(b) updating at least some of the read channel register values from the retrieved values (col. 27 line 55 to col. 28 line 2);

(c) reconfiguring the interface to read data in zone Zb (col. 10 lines 14-31 and col. 14 lines 55-59 wherein the channel 26 configures the interface 22 to read/write data in zone bands); and

(d) reading the target segment (col. 27 line 67 to col. 28 line 2 wherein after updating the read channel registers and reconfigured the interface new data zone band is read/write).

Although Cloke teaches substantial features (discussed above), he fails to explicitly teach the controller is a direct memory access (DMA) controller. Bowes; however, teaches the DMA controller (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill of the art to have the DMA controller in order to alleviate the CPU of the task (col. 1 lines 30-32).

As to claim 7, Cloke teaches the method of claim 6 in which the target segment has a predetermined starting track number, further comprising step of deriving zone identifier Zb from the predetermined starting track number before retrieving step (a) (col. 16 lines 33-60).

As to claim 8, Cloke the method of claim 6 in which the interface includes at least one head (fig. 1A element 19 col. 8 line 19), in which positioning step (c) includes a step (c1) moving the at least one head radially across the disc, the moving step (c1) beginning before retrieving step (a) is complete (col. 8 lines 20-32 wherein the head is used to position the interface prior initiating read/write operations in the new data zone band).

As to claim 9, Cloke teaches the method of claim 8 in which moving step (c1) before retrieving step (a) (col. 8 lines 20-32 wherein the head is used to position the interface prior initiating read/write operations in the new data zone band).

As to claim 10, Cloke teaches the method of claim 6 in which zone Zb has a corresponding data rate Rb that is not in common with zone Za (col. 14 line 67 to col. 15 line 1 wherein the channel frequency will increase in an outward radial direction so that data rate will be different in each zone band), in which position step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate Rb (col. 14 line 60 to col. 15 line 14).

As to claim 11, Cloke teaches the method of claim 6 further comprising steps of:

(e) reconfiguring the interface to read data in zone Zb (col. 10 lines 14-31 and col. 14 lines 55-59 wherein the channel 26 configures the interface 22 to read/write data in zone bands);

(f) receiving a signal from the interface (col. 15 lines 43-48);

(g) deriving several values indicative of the interface's performance in zone Zb from the received signal (col. 22 lines 42-60); and

(h) storing of the derived values in the value table each at a position associated with zone Zb (col. 22 lines 46-50).

As to claim 12, Cloke teaches the method of claim 6 in which the storage system includes an integrate circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the controller (see col. 41 lines 63-65).

As to claim 13, Cloke teaches the method of claim 12 further comprising steps of:

(j) sensing position data from a servo sector via the interface (col. 32 lines 54-65); and

(k) deriving a servo control signal from the sensed position data with the microprocessor during step (b) (col. 41 lines 30-37).

As to claim 14, Cloke teaches the storage system of claim 6 configured to perform the method of claim 6 further comprising a printed circuit board assembly (fig. 1D element 12) including a memory containing the value table (fig. 1D elements 54, 60), the storage system comprising:

a master integrated circuit (IC) containing the microprocessor and the controller (it is obvious to integrate the microprocessor and the controller), the controller being operatively coupled to the memory (fig. 1D elements 32, 54, 60);

a slave IC containing the several read channel registers (fig. 1D element 26); and

a bus coupled between the master IC and the slave IC , the bus controlled by the controller to perform updating (b) (fig. 1D elements 36, 38 wherein the bus 38 couples to the bus 38 through the channel 26).

As to claim 15, Cloke teaches a disc drive (fig. 1D) comprising:

at least one disc (fig. 1D element 14);

an interface configured to read data from the at least one disc (fig 1D element 22 col. 9 lines 28-31);

a memory containing several values indexed by zone identifiers (col. 12 lines 1-9);

a first controller chip containing a microprocessor and a controller, the controller operatively coupled to the memory (fig. 1D element 32, 34);

a first channel chip having several register (fig. 1D element 26 and fig. 4 element 122); and

a bus operatively coupled between the interface and the chips (fig. 1D elements 38, 36 wherein the bus 38 couples to the bus 36 through the channel 26), the bus controllable by the controller to read from the memory and to update several of the registers in response to a Zone transition event (col. 27 lines 44 to col. 28 lines 2).

Although Cloke teaches substantial features (discussed above), he fails to explicitly teach the controller is a direct memory access (DMA) controller. Bowes; however, teaches the DMA controller (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill

of the art to have the DMA controller in order to alleviate the CPU of the task (col. 1 lines 30-32).

As to claim 20, Cloke teaches a controller (fig. 1D element 32) but he fails to explicitly teach a direct memory access apparatus. Bowes; however, teaches the direct memory access apparatus (fig. 2A element 222). It would have been obvious to a person of ordinary skill in skill of the art to have the direct memory access apparatus in order to alleviate the CPU of the task (col. 1 lines 30-32).

***Response to Arguments***

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 571 272-4153. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Nguyen
Patent Examiner
Group Art Unit 2182

10/25/2004

KIM HUYNH
PRIMARY EXAMINER
10/29/04